Notice of Allowability	Application No.	Applicant(s)	
	09/531,397	BALLANTYNE, JOSEPH C.	
	Examiner	Art Unit	
	Syed J. Ali	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed August 22, 2005*.

2. ☒ The allowed claim(s) is/are *34,35,38-40,43-45 and 48, renumbered as claims 1-9*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☒ to Paper No./Mail Date *April 3, 2003*.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MENG-AL T. AN
SUPERVISORY PATENT [illegible]

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Bill Klein (Reg. No. 43,719) on September 8, 2005.

2. **The application has been amended as follows:**

Replace claim 34 as follows:

A computer-readable medium having computer-executable instructions for performing real-time execution-thread switching comprising:

issuing a first non-maskable interrupt from a counter to an interrupt controller when the counter turns over;

in response to receiving the first non-maskable interrupt, issuing a second non-maskable interrupt from the interrupt controller to a central processing unit;

in an interrupt service routine that services the second non-maskable interrupt,

saving a first execution thread's current state information, wherein the first execution thread is an application-level-code execution thread that does not execute in a most-privileged CPU mode, and wherein the first execution thread's

current state information includes stack data, processor data, and floating point-unit data;

setting the counter to specify when the counter will turn over again;

restoring previously stored state information pertaining to a second execution thread, wherein the second execution thread is an application-level-code execution thread that does not execute in a most-privileged CPU mode, and wherein the previously stored state information pertaining to the second execution thread includes stack data, processor data, and floating-point-unit data; and

after execution of the interrupt service routine has finished, executing the second execution thread such that the interrupt service routine that services the second non-maskable interrupt minimizes overhead associated with switching thread execution from the first thread to the second thread.

Cancel claims 36-37.

Replace claim 39 as follows:

A method for performing real-time execution-thread switching comprising:

issuing a first non-maskable interrupt from a counter to an interrupt controller when the counter turns over;

in response to receiving the first non-maskable interrupt, issuing a second non-maskable interrupt from the interrupt controller to a central processing unit;

in an interrupt service routine that services the second non-maskable interrupt,

saving a first execution thread's current state information, wherein the first execution thread is an application-level-code execution thread that does not execute in a most-privileged CPU mode, and wherein the first execution thread's current state information includes stack data, processor data, and floating point-unit data;

setting the counter to specify when the counter will turn over again;

restoring previously stored state information pertaining to a second execution thread, wherein the second execution thread is an application-level-code execution thread that does not execute in a most-privileged CPU mode, and wherein the previously stored state information pertaining to the second execution thread includes stack data, processor data, and floating-point-unit data; and

after execution of the interrupt service routine has finished, executing the second execution thread such that the interrupt service routine that services the second non-maskable interrupt minimizes overhead associated with switching thread execution from the first thread to the second thread.

Cancel claims 41-42.

Replace claim 44 as follows:

A system for performing real-time execution-thread switching comprising:

means for issuing a first non-maskable interrupt from a counter to an interrupt controller when the counter turns over;

means for issuing, in response to receiving the first non-maskable interrupt, a second non-maskable interrupt from the interrupt controller to a central processing unit;

interrupt-service-routine means for servicing the second non-maskable interrupt, including

means for saving a first execution thread's current state information, wherein the first execution thread is an application-level-code execution thread that does not execute in a most-privileged CPU mode, and wherein the first execution thread's current state information includes stack data, processor data, and floating point-unit data;

means for setting the counter to specify when the counter will turn over again;

means for restoring previously stored state information pertaining to a second execution thread, wherein the second execution thread is an application-level-code execution thread that does not execute in a most-privileged CPU mode, and wherein the previously stored state information pertaining to the second execution thread includes stack data, processor data, and floating-point-unit data; and

means for executing the second execution thread, after the interrupt-service-routine means services the second non-maskable interrupt, such that the interrupt-service-routine means minimizes overhead associated with switching thread execution from the first thread to the second thread.

Cancel claims 46-47.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J. Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T. An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
September 8, 2005

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